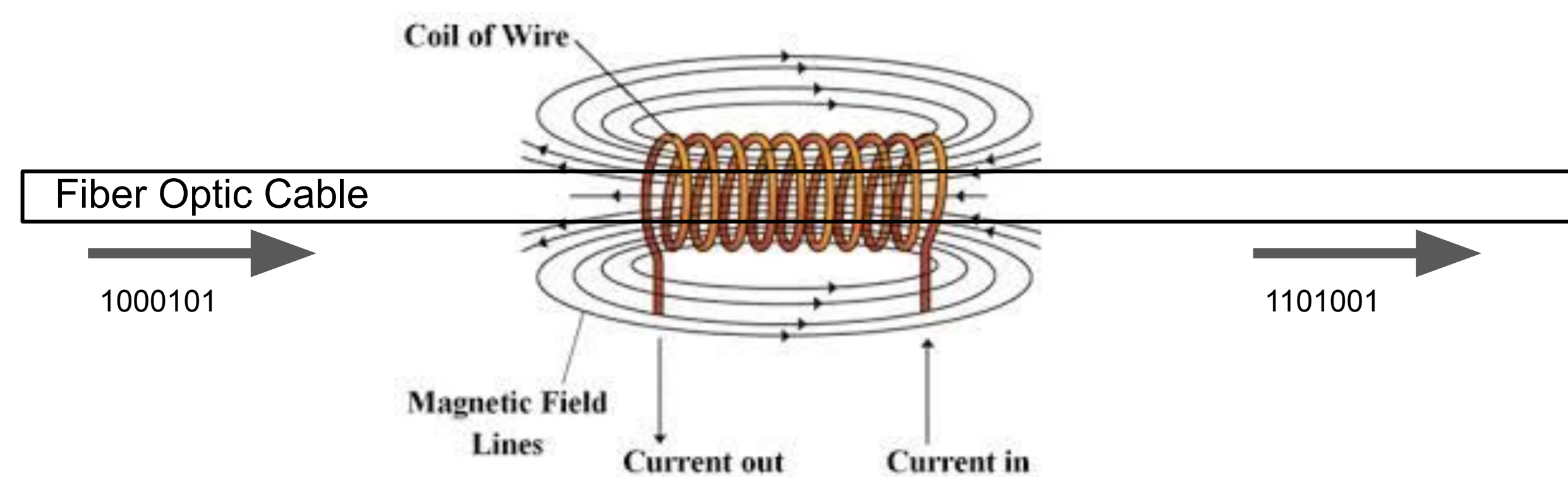# High Speed Magnetic Field Generator (HS-MFG)
SDMay20-39

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Zack Higgs - Team Lead
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Harel Cohen - Hardware Lead
Ben Colson - Test Engineer Lead

Professor Mani Mina - Client
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Project Overview

All around us are signals being transmitted to and from us. One of the fastest and most promising method of long-distance data delivery is fiber optics. By sending signals using light that is trapped in glass fiber, we don't have to worry about types of interference that are caused in signal carrying metal wire. Our solution is to develop a HS-MFG which can change, or "refresh," the data sent via these optic fibers without needing to cut the fiber and use slower metal wires.

Requirements

These are the main goals we must achieve for this High Speed Magnetic Field Generator HS-MFG:
Functional Requirements
- High speed magnetic field generator
- 500 Gauss field
- Rise time < 100 ns
Non-Functional Requirements
- Size must be less than 3.5" x 2"
Operating Environment
- Non-hazardous
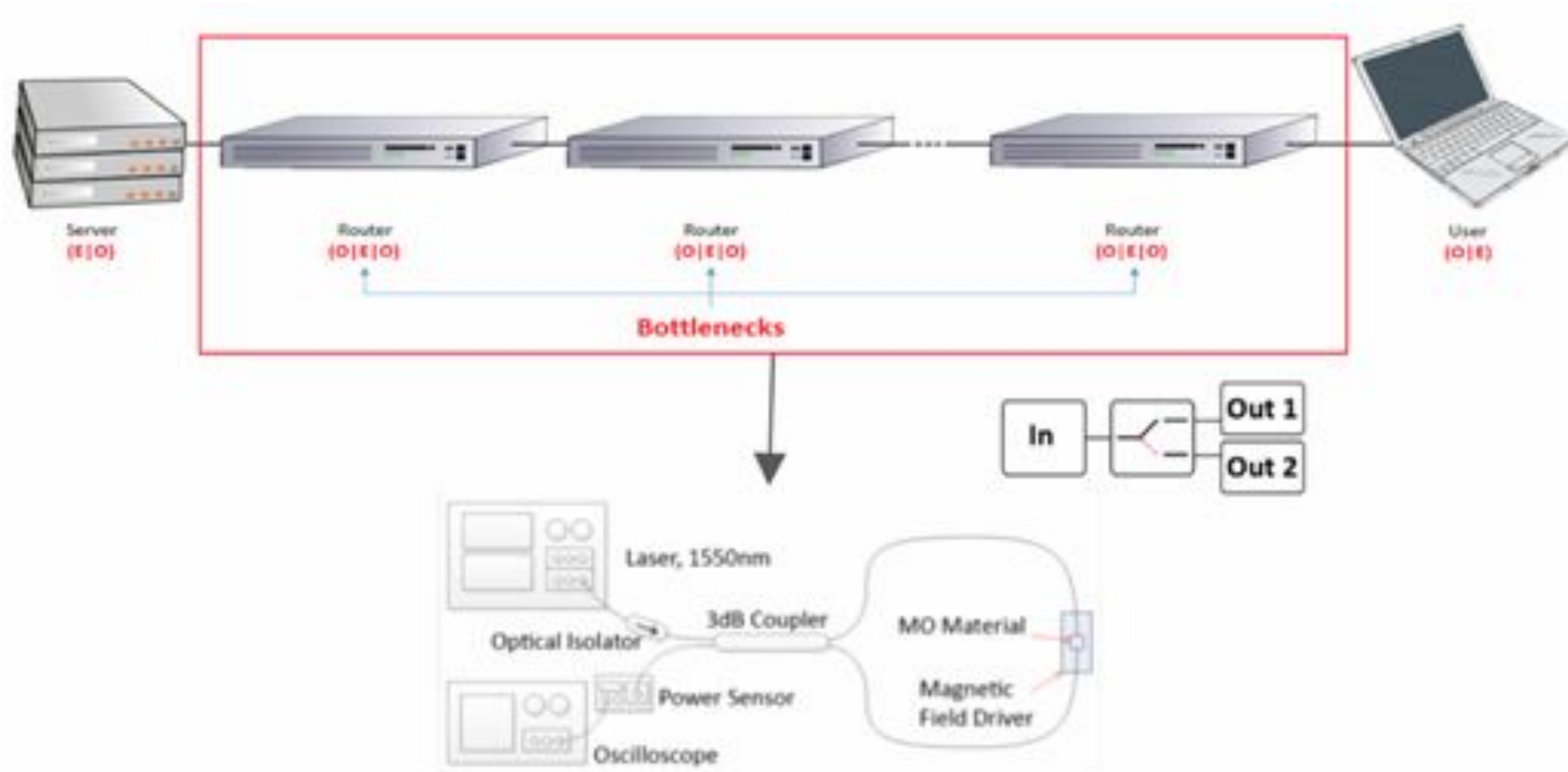- Ensure no electrical interference with device

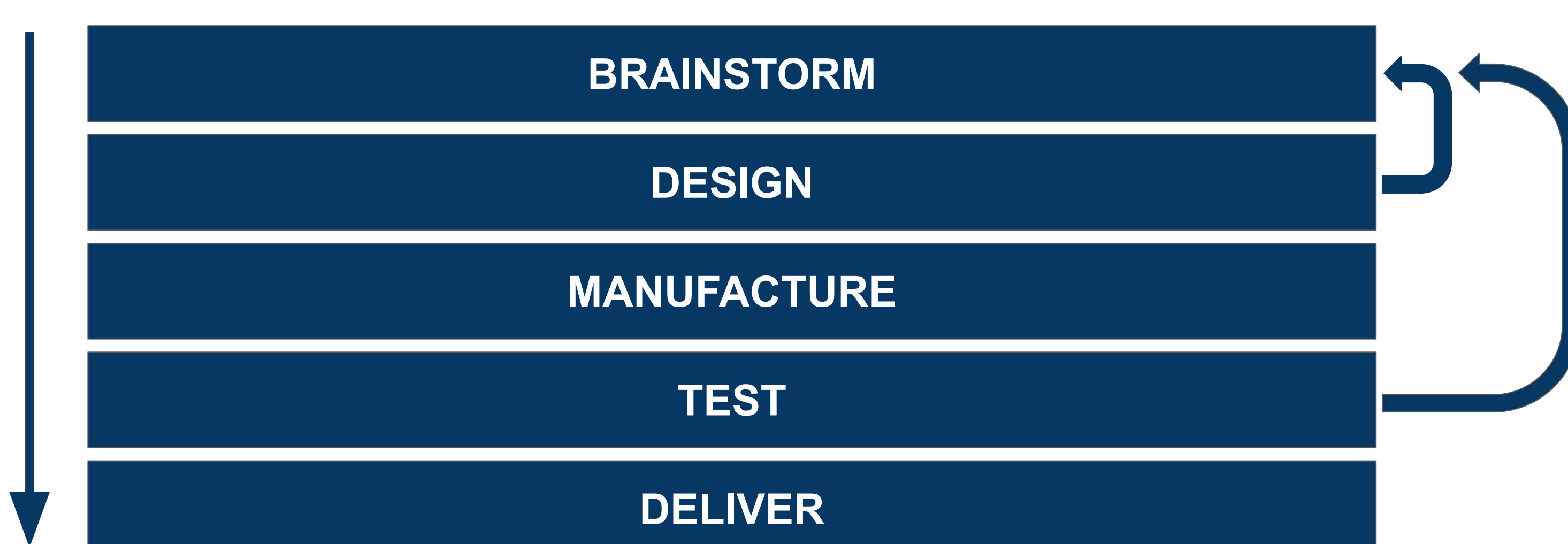## Implementations and Users

Uses
- Implemented into existing networks decrease delay of signal
Users
- Developers of medical/routing equipment
- Consumers of said equipment

Design Approach

- BRAINSTORM
- DESIGN
- MANUFACTURE
- TEST
- DELIVER

Technical Design

The Main Circuit:

Coil
- 5 turns (200pH)
MOSFET
- SIRA28BDP-T1
Capacitor Bank
- Frequency eliminating
- Up to 25V
Boost Converter
- RECOM 12-20V DCDC

Spice simulation of the HS-MFG

Test Circuit Diagram

- Adds daughterboard for quickly testing MOSFETs
- Adds test points for easy probing across
- Adds voltage input boost/buck converter to adjust input voltage for MOSFET

Testing

MOSFET Testing
- Decreased rise time by using the fastest MOSFET tested
Daughter Board
- Allows for fast replacement of MOSFETs
Parasitics
- Simulations and trace-length reduction

Final PCB with Daughter Board   *Final PCB Trace with heavy oscillations*

Future Work

- PCB with no Daughter
  - Covid related final printing
- SCR (Silicon Controlled Rectifier)
- GaN MOS with boost
  - Implementing RECOM after converter
- Continuous lowering of rise time
  - Eventual goal is about 10ns
- Cleaning signals
  - Reduce noise and unwanted spiking